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(54) High voltage semiconductor monolithic device with integrated edge structure and corresponding manufacturing process

(57) A monolithic high-voltage semiconductor device with integrated edge structure of the type provided on a semiconductor material substrate (2) having a first conductivity type and on which are grown a first (5) and second (6) epitaxial layer having the same conductivity type.

The device (1) comprising also a type PN junction (3) including a first diffuse region (4) having a second conductivity type provided inside the first (5) and second (6) epitaxial layers and an edge structure (10) also provided inside the epitaxial layers (5) and (6) and adjacent to the junction (3) including a termination region (12) having a second conductivity type.

The device (1) is characterized in that the edge structure (10) also comprises at least one thin region (13) having a second conductivity type located between the junction (3) and the termination region (12).

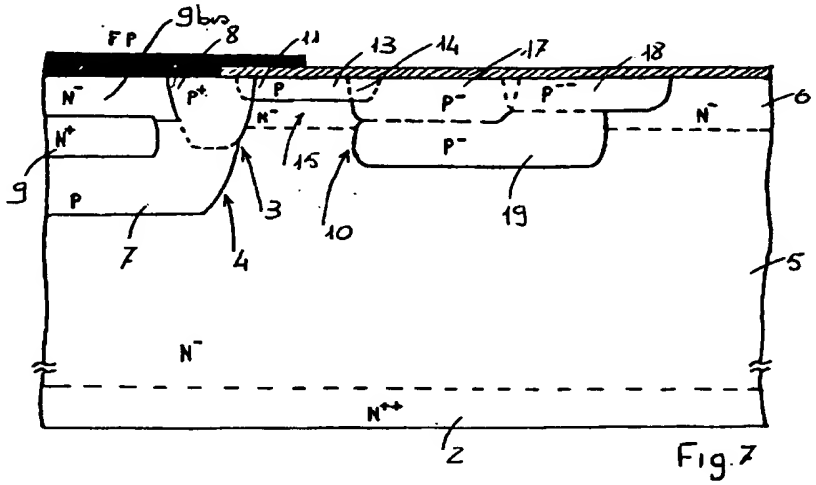

Fig. 7

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Descripti n

The present invention relates to a monolithic high-voltage semiconductor device with integrated edge structure and an to associated manufacturing process.

As known, monolithic high-voltage semiconductor devices comprising type PN planar junctions must withstand high voltages with reverse bias.

A typical example is the base-collector junction of an NPN bipolar transistor.

The larger part of PN junctions provided by planar technology comprise essentially a first semiconductor region, e.g. a diffuse region having a first conductivity type which is formed inside a second semiconductor region, e.g. an epitaxial layer having conductivity of opposite type.

Over these two regions is deposited an insulating oxide layer on which are provided the metallic contacts for electrical connection of the junction.

Under conditions of reverse bias the junction is surrounded by a charge depletion region in which is present an electrical field which does not have uniform distribution.

Indeed, as shown in FIG. 1, opposite the flat portion of the junction the equipotential lines are parallel while opposite the edge portion of the junction, because of the finite dimensions of the latter, the equipotential lines are curved and are much less spaced apart.

This involves raising of the electrical field especially near the surface of the semiconductor device.

This high surface electrical field causes the breakdown voltage of the junction to be less opposite the edge portion than at the flat portion.

To reduce the electrical field in the edge portion there are used different known technical solutions.

A common objective of these techniques is essentially that of modifying the dimensions of the depletion region so as to prevent local increases in the electrical field from causing premature junction breakdown.

A first solution of the prior art to satisfy this requirement calls for provision of so-called metallic field plates which are formed by extending the metallic contact of the diffuse regions over the insulation oxide layer as shown in FIG. 2.

The metallic field plate, by acting as a shield, forces the equipotential lines to extend in a wider portion of the semiconductor device to aid reduction of the surface electrical field and consequent increase in the breakdown voltage of the junction edge portion.

Although advantageous in some ways this first technical solution of the prior art exhibits the shortcoming that at the edges of the metallic field plate the shielding action decreases with consequent increase in the surface electrical field.

A second solution of the prior art is described in US patent no. 4,667,393 of the same applicant which suggests providing near the junction edge portion an edge structure comprising one or more so-called high-resistivity rings as shown in FIG. 3.

The depletion region is thus extended into a broader portion of the semiconductor device to broaden the space charge distribution with resulting decrease in the surface electrical field.

Specifically the rings are provided inside the epitaxial layer by means of implantation and diffusion of a dopant material having conductivity type opposite that of the epitaxial layer and specifically type P-.

By controlling the amount of implanted material and the diffusion process it is possible to achieve the desired resistivity.

When the semiconductor device must withstand high voltages there are provided two or more concentric rings with resistivity decreasing from the inside outward.

However, small ring junction depth to epitaxial layer thickness ratios are responsible for rather high surface electrical field values hence sensitive to the charges present near the device surface (moving charges and charges located at the interface between the insulating oxide and the silicon).

Local variations in the electrical field due to these charges can generate so-called walk out/walk in phenomena or conduction of channeled charges which overall make the edge structure unsteady and precarious.

As shown in FIG. 4, by increasing the ring junction depth to epitaxial layer thickness ratio there are obtained rings with greater curve radii which improve the uniformity of the depletion region and lower the surface electrical field values.

Thus there is provided another technical solution of the prior art, denominated "deep ring technique", capable of ensuring better stability of the edge structure.

It is noted that this technique is based on the important result that the junction breakdown voltage depends heavily on the quantity $\Delta X=Xj2-Xj1$ where Xj1 is the junction depth for the junction to be protected while Xj2 is the junction depth of a so-called termination region incorporating the rings provided by the above mentioned technique as shown in FIG. 5.

In the presence of termination regions with non-unitary edge efficiency, upon increase in the positive quantity ΔX the breakdown voltage of the junction to be protected also increases.

The edge structures provided in this manner have the advantage of making breakdown of the junction to be protected independent of the diffuse region since the breakdown takes place in the termination region.

Provision of termination regions with high junction depth involves the use of fast diffusers or long or high-temperature diffusion cycles in the case of slow diffusers.

This makes the edge structure integration process very costly especially in the case of slow diffusers.

The technical problem underlying the present invention is to provide a monolithic semiconductor device with integrated edge structure especially efficient and economical to manufacture.

The solution idea underlying the present invention

is to place between a junction to be protected and a termination region a thin region of appropriate thickness and doping so as to achieve extension of the junction to be protected while simultaneously reducing its depth.

The technical problem is solved by a device of the type indicated above and defined in the characterizing part of claims 1 to 11 annexed hereto.

The technical problem is also solved by a process for manufacture of the above mentioned device in accordance with claim 12.

The characteristics and advantages of the device and process in accordance with the present invention are set forth in the description of an embodiment thereof given below by way of non-limiting example with reference to the annexed drawings.

In the drawings:

FIG. 1 shows a vertical cross section in enlarged scale of a planar junction,

FIGS. 2 to 5 show vertical cross sections in enlarged scale of different embodiments in accordance with the prior art of an edge structure associated with the planar junction shown in FIG. 1,

FIG. 6 shows a vertical cross section in enlarged scale of a high-voltage semiconductor device with incorporated edge structure provided in accordance with the present invention,

FIG. 7 shows the device of FIG. 7 with incorporated edge structure represented in a second and more general embodiment in accordance with the present invention, and

FIGS. 8 to 10 show different trends of the equipotential lines inside the device in accordance with the present invention.

With reference to the figures reference number 1 indicates as a whole and schematically a monolithic high-voltage semiconductor device provided in accordance with the present invention with an integrated edge structure.

The device 1 shown in FIG. 6 is achieved starting from a substrate 2 of semiconductor material, e.g. silicon, having a first type of conductivity and in particular type N++ on which are grown a first 5 and a second 6 epitaxial layer having the same type of conductivity and in particular type N-.

The first epitaxial layer 5 has a high resistivity and a considerable thickness to ensure voltage tightness of the device 1.

In addition the device 1 comprises a junction 3 provided through a first diffuse region 4 having a second type of conductivity and in particular type P which is formed in the first 5 and second 6 epitaxial layers.

Specifically the first diffuse region 4 comprises a first buried region 7 having conductivity of the second type and in particular type P and a deep region 8 having conductivity of the same type and in particular type P+.

The deep region 8 contacts laterally the first buried region 7 connecting it to the surface of the device 1.

It is noted that in the case of VIPower™ high voltage devices (breakdown voltage: 1000V-20000) the first buried region 7 should have a junction depth around 1/4 to 1/3 the residual thickness of the first epitaxial layer 5 underlying the region.

Inside the first diffuse region 4 is included a second diffuse region 9 having conductivity of the first type and in particular type N+ which delimits below a portion 9bis of the epitaxial layer 6 designed to received a circuitry operating at low and/or high voltage.

The first diffuse region 4 forms an annular insulating region enclosing the second diffuse region 9 and the portion 9bis of the epitaxial layer 6 to isolate it completely from the rest of the device 1.

Again with reference to FIG. 6 the device 1 also comprises an edge structure 10 provided inside the epitaxial layers 5 and 6 and in part overlying a portion of edge 11 of the junction 3.

This edge structure 10 comprises at least one termination region 12 having conductivity of the second type and in particular type P- and at least one thin region 13 having the same type of conductivity and in particular type P located between the edge portion 11 of the junction 3 and the termination region 12.

Specifically the thin region 13 is provided in the second epitaxial layer 6 and is partly overlaid on the portion 11 of the junction 3 and partly overlaid on a portion 14 of the termination region 12.

In addition this thin region 13 is provided with appropriate thickness and doping to achieve an extension of the junction 3 while reducing its depth at the same time.

The thin region 13 can also be provided with an inconstant and gradually decreasing resistivity as it approaches the termination region 12.

Specifically the thin region 13 must be less deep than the termination region 12 so as to make more significant the difference between the junction depth of the termination region 12 and the junction depth of the outermost region of the junction 3.

The thin region 13 is also capable of decoupling the electrical field created along the edge portion 11 of the junction 3 from the electrical field created along the edge portion 14 of the termination region 12 overlaid on the thin region 13.

This decoupling occurs when the electrical field component parallel to a junction 15 formed by the thin region 13 and the second epitaxial layer 6 reaches virtually null values in the zone of the epitaxial layer 6 underlying the junction 15 for a depth dependent upon the ratio of the dope concentrations present in the thin region 13 to those present in the epitaxial layers 5 and/or 6.

The width of the thin region 13 also depends on the ratio of its dopant concentration to the dopant concen-

tration present in the edge portion 14 of the termination region 12.

From another viewpoint effectiv decoupling of the electrical field is achieved when the structure of the termination region 12 is fixed and the dose and extension of the thin region 13 are combined in such a manner as to eliminate the critical nature of the gradient of the equipotential lines respectively on the edge portion 14 of the termination region 12 and on the edge portion 11 of the junction 3, whence can derive edge breakdown of the device 1.

It is noted that if the termination region 12 is provided using material with high diffusivity such as e.g. aluminium while the same region 12 includes a third diffuse region 16 with high resistivity having conductivity of the second type and in particular type P- as shown in FIG. 6.

For termination regions provided in this manner and hence very deep the thin region 13 can comprise at least two diffuse regions having type P conductivity and formed on the two epitaxial layers 5 and 6 in such a manner as to better protect the junction 3.

If the termination region 12 is provided using a material with lower diffusivity, e.g. boron, the termination region 12 can be formed from a fourth 17 and a fifth 18 diffuse regions which have greater junction depth than the edge portion 11 of the junction 3.

To further increase this junction depth beneath the two diffuse regions 17 and 18 there can be provided a second buried region 19 as shown in FIG. 7.

The three regions exhibit high resistivity and conductivity of the second type.

Specifically for the example shown in the figure the fourth diffuse region 17 and the second buried region 19 exhibit type P- conductivity while the fifth diffuse region 18 has type P-- conductivity.

Lastly the device 1 comprises a layer of insulating oxide 20 located on the surface on which is provided a metallic region 21 for contact of the junction 3 which extends not beyond the portion 11 of the junction.

There are now described the steps of the process leading to production of the device 1.

The integration process begins with growth of the first epitaxial layer 5 on the substrate 2.

In this first epitaxial layer 5 is provided by implantation and successive diffusion heat treatment the buried region 7.

Successively, opposite this buried region 7, is provided by means of implantation and successive diffusion heat treatment the second diffuse region 9.

On the first epitaxial layer 5 is then grown the second epitaxial layer 6 in which is implanted and successively diffuse the deep region 8 to permit electrical continuity with the buried region 7.

The steps thus far described provide for standard production of the diffuse and insulated regions typical of VIPower™ devices which use the junction insulation technique for the various components making up the circuitry incorporated in the portion 9bis of the second epitaxial layer 6.

After completion of these steps one proceeds to provision of the edge structure 10.

The thin region 13 which ensures electrical continuity between the junction 3 and the termination region 12 is provided in an intermediate step between formation of the second epitaxial layer 6 and formation of the deep region 8 by means of implantation and successive dedicated diffusion heat treatment.

As an alternative the thin region 13 is formed in successive steps by using implants and heat cycles necessary for provision of the various components making up the circuitry incorporated in the portion 9bis of the second epitaxial layer 6 and hence not explicitly dedicated to provision of the thin region 13.

For provision of the thin region 13 there can also be used variable transparency solutions.

The integration process of the device 1 continues with provision of the termination region 12.

As concerns this region also different process variants are possible.

Specifically if a high-diffusivity dopant material is used the termination region 12 is formed by implantation and successive diffusion heat treatment of the third diffuse region 16.

If the material used has lower diffusivity the termination region 12 is formed by implantation and successive diffusion heat treatment of one or more regions, e.g. the fourth 17 or fifth 18 diffuse region so that it is always deeper than the thin region 13 in the part contiguous therewith.

In this regard it is possible to use the same heat treatment used to diffuse the deep region 8 after use of dedicated implantation in the desired regions.

Furthermore if it is desired to improve the overall characteristics of the edge structure 10 there can be achieved e.g. relatively deep diffuse regions using the first epitaxial layer 5.

Indeed, in accordance with the criteria of the prior art, by dedicated implantation and successive diffusion heat treatment to be performed on this first epitaxial layer 5 there can be provided one or more buried regions such as e.g. the second buried region 19.

The only condition to be observed for this purpose is that after completion of the edge structure electrical continuity be assured between the regions integrated respectively on the first and second epitaxial layers (diffuse regions 17 and 18 and second buried region 19).

For the termination regions of the above described type the known variable transparency technique can be used by appropriately modifying the layouts defining formation of the diffuse regions to achieve more elaborate edge structures.

After completion of the termination region 12 the integration process of the device 1 proceeds in accordanc with the known integrated power device manufacturing techniques.

In conclusion the device 1 in accordance with the present invention comprises an edge structure 10 which

overall exhibits the characteristics called for by integration of termination regions in accordance with the above mentioned known techniques while not necessarily having recourse to integration of termination regions with extremely deep junctions.

An example of an edge structure comprising a termination region provided as in FIG. 7 was simulated by including provision of the thin region 13 in the intermediate step between formation of the second epitaxial layer 6 and formation of the deep region 8.

FIG. 8 shows the simulated edge structure with hatching while the junction portion belonging to the thin region 13 is shown with crosses.

In the same figure are also shown the equipotential lines spaced 50V apart, e.g. for the case of a substrate dimensioned for 1500V and biased at this voltage.

It is important to note that near the thin region 13 the equipotential lines remain virtually parallel with the surface of the device 1 while the potential increases mainly beneath the junction 3 to ensure breakdown opposite its flat portion.

In figures 9 to 9b are reproduced in detail the simulated behaviors of the equipotential lines in the thin region 13.

The three charts concern the same edge structure in which, from top to bottom, the width of the thin region 13 is that specified, half or absent.

From the figure it appears clearly that the equipotential lines tend rapidly to deflect toward the edge portion 14 of the termination region 12 where the extension of the thin region 13 is reduced to less than 30μm.

In parallel the location of the maximum electrical field passes from the corner of the junction 3 to the transition point between the thin region 13 and the termination region 12 to procure breakage of the edge structure as shown by a crossed line.

Again, since behind the portion 14 of the termination region 12 the electrical field is reduced the depletion region formed outside the junction 3 when it is reverse biased essentially affects the termination region 12 without involving the thin region 13.

Marginally to these simulations it was also verified that the presence of a metallic field plate has no influence on the behavior of the potential in the thin region 13 as may be inferred by comparison of FIG. 8 with FIG. 10 for an edge structure having a short field plate.

Finally, recourse to the thin region 13 appears to be a valid option because it allows reduction of the overall extension of the termination region 12 while keeping its edge efficiency.

Claims

1. Monolithic high-voltage semiconductor device with integrated edge structure of the type provided on a semiconductor material substrate (2) having a first conductivity type and on which are grown a first (5) and a second (6) epitaxial layer having the same conductivity type as well as comprising a type PN junction (3) including a first diffuse region (4) having a second conductivity type provided inside the first (5) and second (6) epitaxial layers and an edge structure (10) also provided inside the epitaxial layers (5) and (6) and adjacent to the junction (3) including a termination region (12) having a second conductivity type and characterized in that said edge structure (10) also comprises at least one thin region (13) having a second conductivity type located between the junction (3) and the termination region (12).

2. Device in accordance with claim 1 and characterized in that the thin region (13) is provided inside the second epitaxial layer (6).

3. Device in accordance with claim 2 and characterized in that the thin region (13) is partly overlaid on an edge portion (11) of the junction (3).

4. Device in accordance with claim 3 and characterized in that the thin region (13) is partly overlaid on an edge portion (14) of the termination region (12).

5. Device in accordance with claim 1 and characterized in that the thin region (13) has a type P conductivity.

6. Device in accordance with claim 5 and characterized in that the thin region (13) is thinner than the termination region (12).

7. Device in accordance with claim 6 and characterized in that the thin region (13) has a length and resistivity dependent upon the dopant material concentration of the regions adjacent thereto.

8. Device in accordance with claim 7 and characterized in that the resistivity of the thin region (13) is less than that of the termination region (12).

9. Device in accordance with claim 8 and characterized in that the resistivity of the thin region (13) is greater than that of the edge portion (11) of the junction (3).

10. Device in accordance with claim 6 and characterized in that the thin region (13) has inconstant resistivity.

11. Device in accordance with claim 1 and characterized in that the thin region (13) includes at least two diffuse regions having conductivity of the second type and provided inside the first (5) and the second (6) epitaxial layers.

12. Process for the manufacture of a monolithic high-voltage semiconductor device with integrated edge structure and provided on a semiconductor material

substrate (2) having a first conductivity type and on which are grown a first (5) and a second (6) epitaxial layer having the same conductivity type with said device comprising also a type PN junction (3) including a first diffuse region (4) having a second conductivity type provided inside the first (5) and second (6) epitaxial layer and an edge structure (10) provided inside the epitaxial layers (5) and (6) and adjacent to the junction (3) including a termination region (12) having a second conductivity type and characterized in that it calls for a step of implantation and successive diffusion of at least one thin region (13) having a second conductivity type called for inside the second epitaxial layer (6) between the junction (3) and the termination region (12).

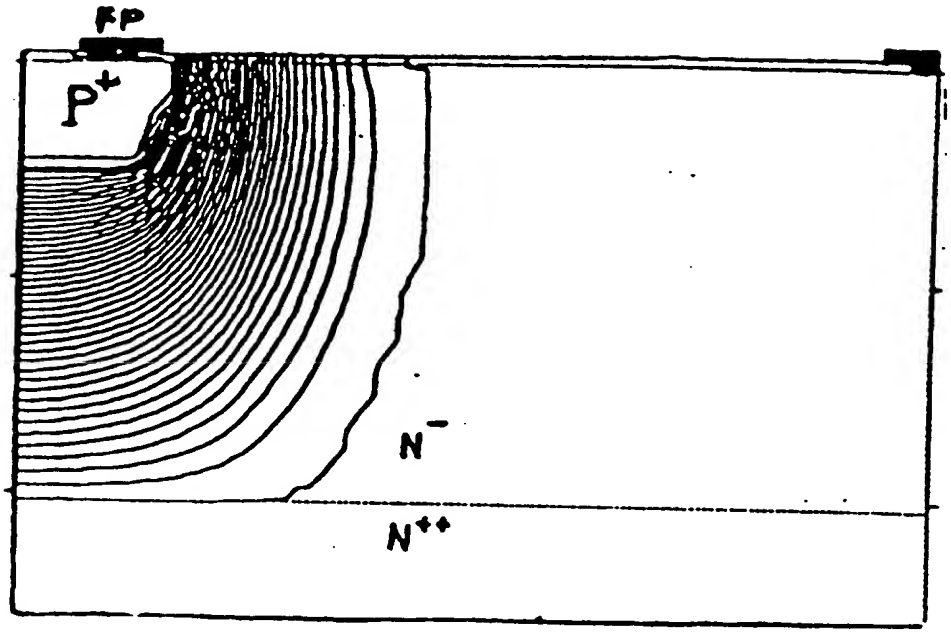


Fig. 1

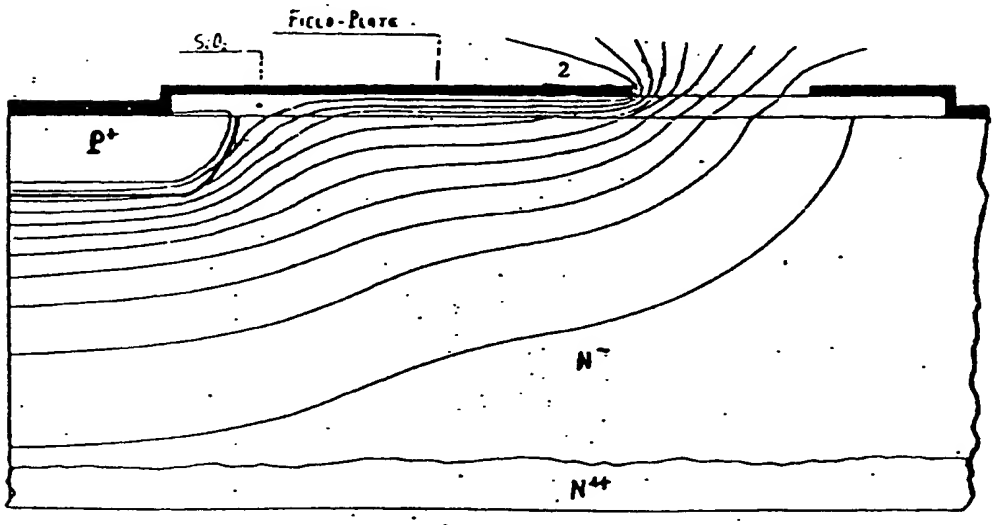


Fig. 2

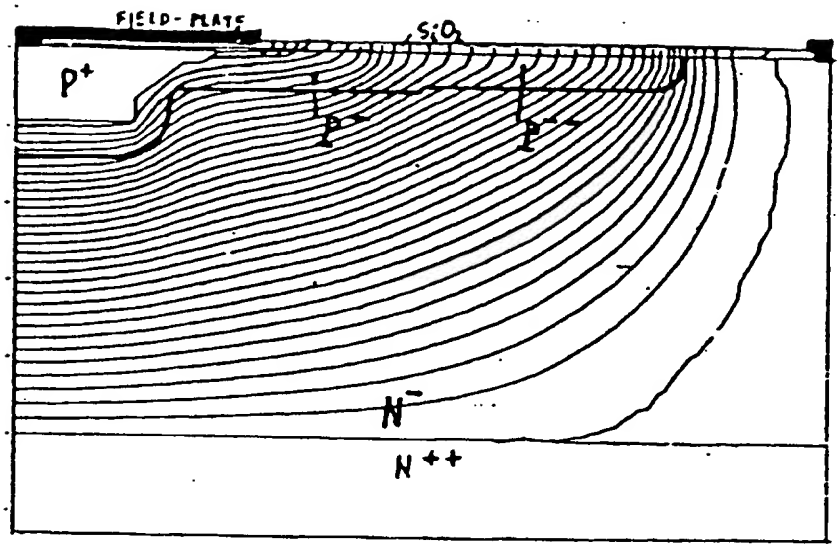


Fig.3

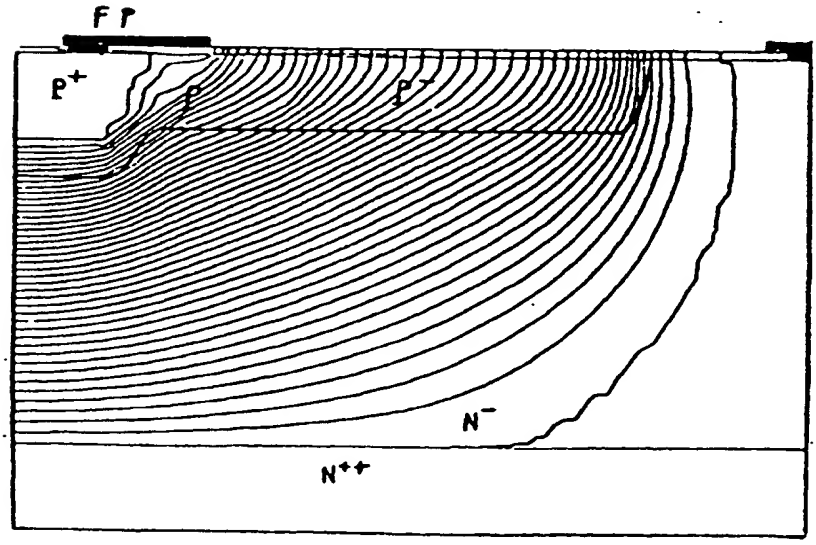


Fig.4

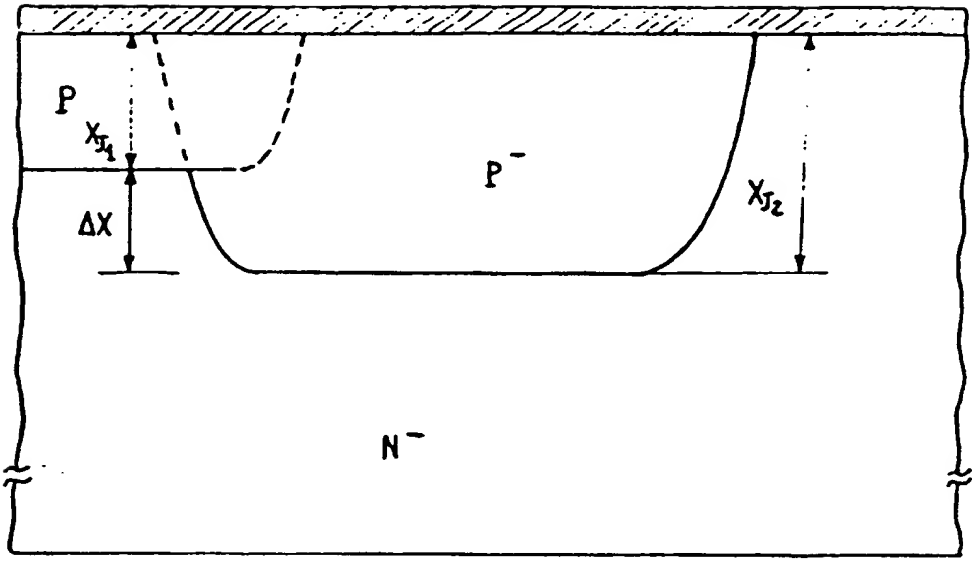


Fig.5

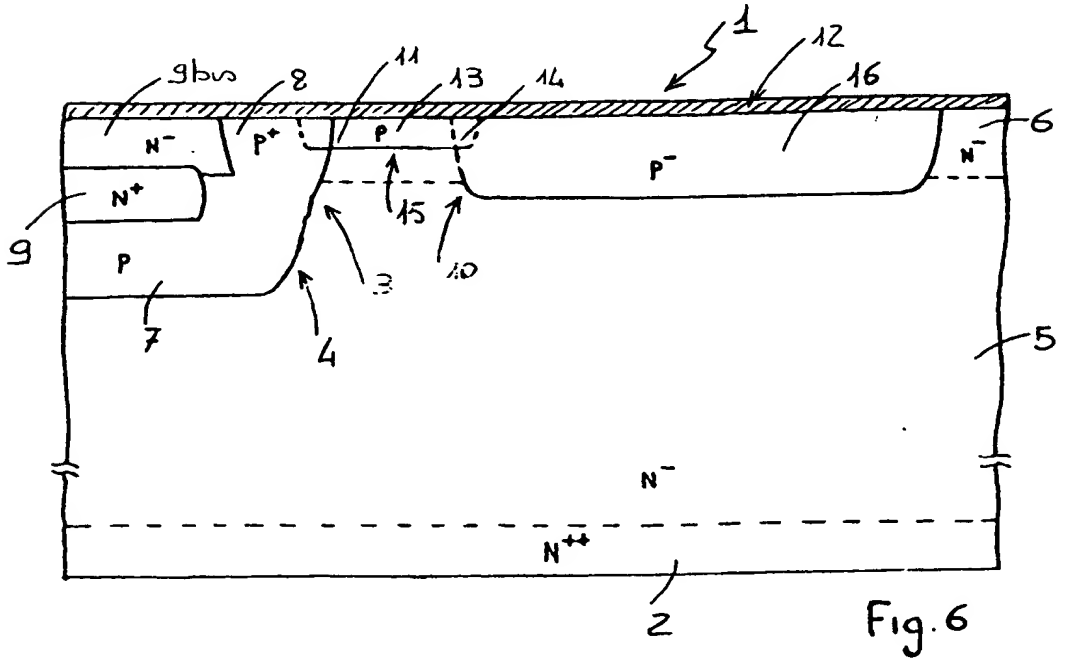
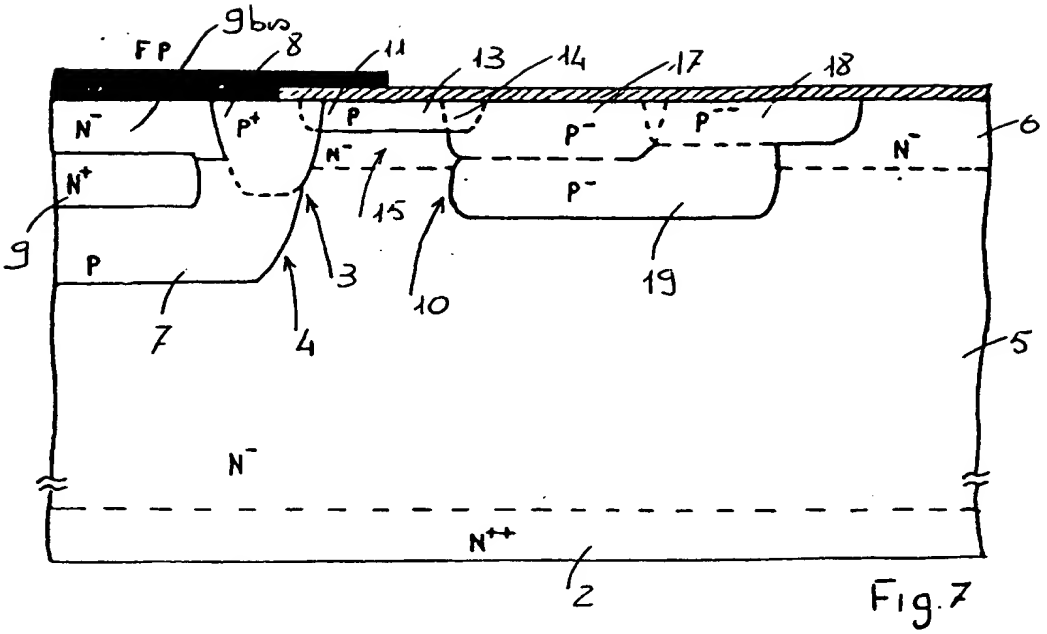


Fig.6


FP
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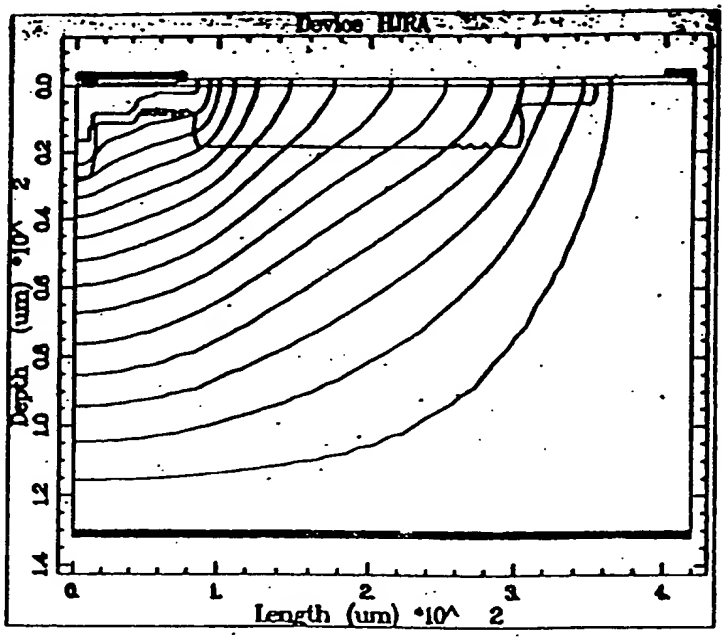
11
13
14
17
18
N⁻
P⁺
P
P⁻
P⁻⁻
N⁻
6
N⁺
N⁻
15
P⁻
9
P
3
10
19
7
4
5
N⁻
N⁺⁺
2

Fig.7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1.0
1.2
1.4
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2
3
4
Length (um) *10^ 2

Fig 8

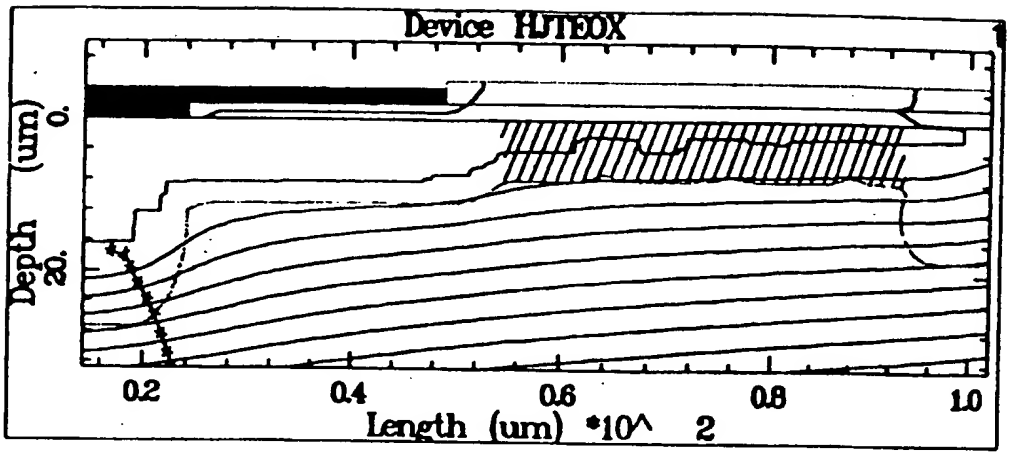
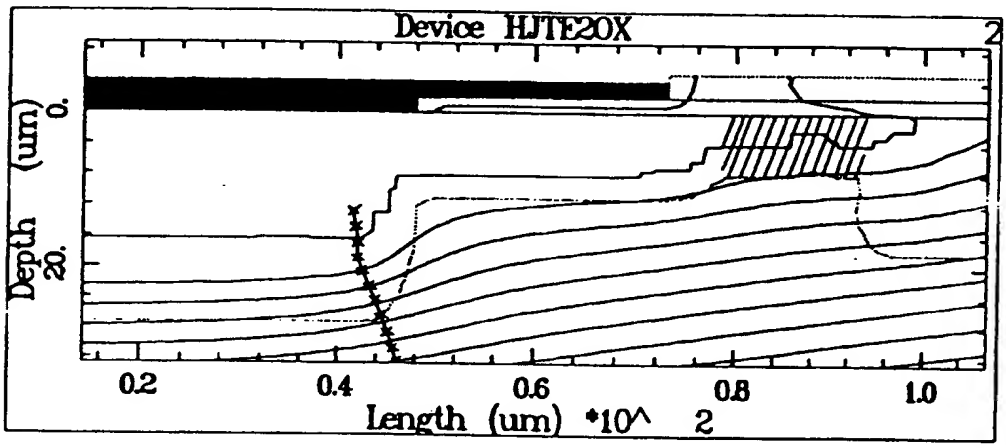


Fig. 9



impianto di tipo p-shallow

Fig. 9a

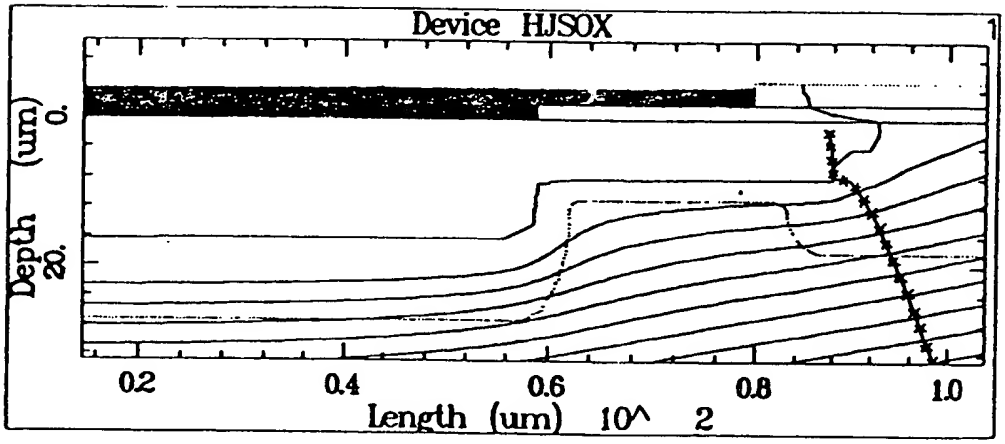
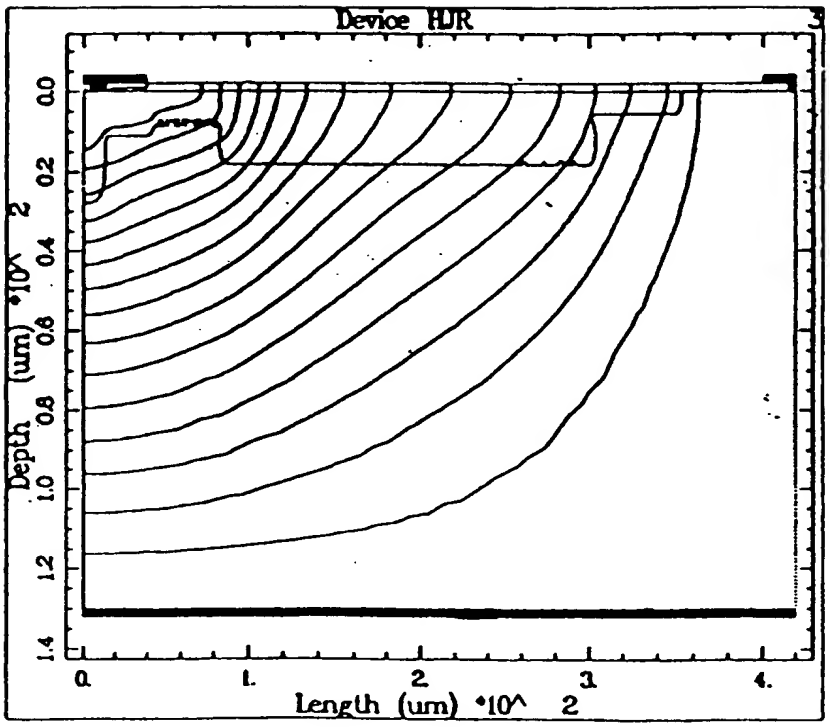


Fig. 9b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0.4
0.6
0.8
1.0
1.2
1.4
0.
1.
2.
3.
4.
Length (um) *10^ 2

Fig 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0343

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 015 no. 371 (E-1113) ,18 September 1991 & JP-A-03 147331 (SHINDENGEN ELECTRIC MFG CO LTD) 24 June 1991, * abstract * ---	1,3-7,9, 12	H01L23/00 H01L29/08 H01L29/06
X	PATENT ABSTRACTS OF JAPAN vol. 008 no. 036 (E-227) ,16 February 1984 & JP-A-58 192369 (TOKYO SHIBAURA DENKI KK) 9 November 1983, * abstract * ---	1,3-7,9, 12	
D,A	US-A-4 667 393 (FERLA GIUSEPPE ET AL) 26 May 1987 * the whole document * ---	1-3,5,9, 10,12	
A	GB-A-2 134 705 (PHILIPS ELECTRONIC ASSOCIATED) 15 August 1984 * the whole document * ---	1,11	
A	EP-A-0 571 027 (PHILIPS ELECTRONICS NV) 24 November 1993 * abstract; figure 1 * -----	1,8	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 December 1995	Mimoun, B

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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